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Design of A Novel Low Power Dynamic Comparator Using 90nm CMOS Technology

Binu C. Pillai[1], Binoshi Samuvel[1]

Assistant Professor, Dept of Electronics and Communication Engineering, Amal Jyothi College of Engineering, Kanjirappally, India[1]

Abstract: This paper describes design of a low power dynamic comparator which can be used in the implementation of high speed ADC. It uses a dual input single output differential amplifier as a latch stage instead of a back to back inverter. This design efficiently removes the noise at the input. Compare to existing comparators this proposed model has higher speed, lower power dissipation and higher immunity to noise. The schematic simulation has been done in Cadence® Virtuoso Analog Design Environment using GPDK 90nm technology. The layout has been done in Cadence® Virtuoso Layout XL Design Environment.

Keywords: CMOS, Comparator, Cadence, Latch.

I. INTRODUCTION

Comparators have a variety of uses, including: Polarity identification, 1-bit analog to digital conversion, switch driving, wave generation and pulse edge generation. It is largely used in A/D converters. The performance of the ADC depends on the inter-stage gain amplifiers and comparators. Dynamic comparator have high speed, consumes less power and provide full swing digital output level. Hence they are widely used in today's ADCs. A comparator is basically a circuit which compares an analog signal with a reference signal and gives a corresponding binary output. Pre-amplifier based comparators has the drawback of higher offset voltage. This problem is overcome with a dynamic comparator which makes a comparison once every clock cycle and uses much less offset voltage.

II. ARCHITECTURE

A. Pre-amplifier Based Comparator

Fig.1. shows a block diagram of general type CMOS comparator. It consists of three stages viz. pre-amplifier, a decision making stage and an output buffer. The pre-amp improves the comparator sensitivity by amplifying the input signal and also isolating the input of the comparator from the kick back noise. The decision making stage is a positive feedback section and finds which input signal is larger. The buffer stage amplifies it and outputs a digital signal.

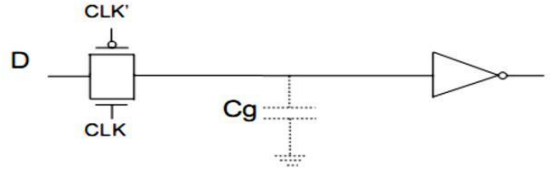

Fig.1. Block diagram of pre-amplifier based comparator

B. Dynamic Latch

A dynamic latch is a simple memory unit that stores the charge on the gate capacitance of the inverter. The latch is driven by a clock. When clock in high (clk =1) the transmission gate is closed, and the inverter is directly connected to the input. When clock is low (clk =0) the transmission gate is open and output of the inverter is depends on the node. Fig.2. shows a simple dynamic latch circuit.

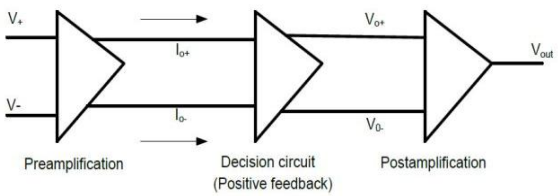

Fig.2. Dynamic Latch

C. Pass Transistor

Pass transistor logic (PTL) is used in design of integrated circuits. PTL reduces the total number of transistors used to form different logic gates, by eliminating redundant transistors. Instead of acting as switches connected directly to supply voltage, transistors are used as switches to pass logic levels between nodes of a circuit. The pass transistor is driven by a periodic signal (clock) and thus we have logic '1' transfer and logic '0' transfer on basis of the clock signal.

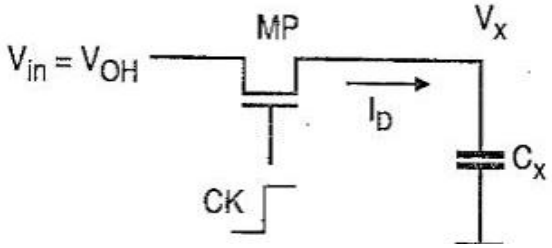

Fig.3. Pass Transistor

The pass transistor MP is an NMOS device, but could also be implemented with a transmission gate TG.

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Cx represents the equivalent capacitance of the input gate of the second NMOS device (part of an inverter or logic gate) as well as the PN junction capacitance of MP's drain (source) If Vin is high (say VOH), then MP will allow current to flow into Cx, charging it up to Vdd – Vtn (assume CK up level is Vdd). If Vin is low (say GND), then MP will allow current to flow out of Cx, discharging it to GND

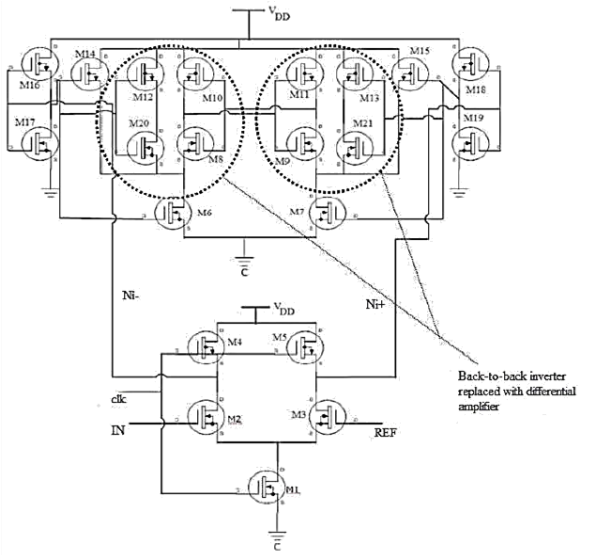

Fig.4. Comparator Circuit

D. Comparator Circuit

In the proposed comparator the back-to-back latch stage in existing comparators is replaced with back-to-back dual input single output differential amplifier. The conventional latch is basically an inverter and the modification has many advantages over it. The main advantages are that it had higher immunity to environmental noise and has better CMRR. Differential signaling also increases the maximum achievable voltage swings. It also provides simpler biasing and higher linearity. Fig.4. shows circuit diagram of the comparator.

Operation:

During reset phase (clk= 0V), PMOS transistor M4 and M5 turn on and they charge Ni node voltages to VDD. And Hence NMOS transistors M17 and M19 turns on and discharges Ni' nodes voltages to GND. Then M14, M15 and PMOS transistors of differential amplifier blocks M12 and M13 turns on, NMOS transistors of differential amplifier block M8, M9 and M6, M7 turns off. The out nodes are charges to VDD. During evaluation phase (clk= VDD), the Ni node capacitances are discharged from VDD to GND in a rate which is proportional to the input voltages. At a certain voltage of Ni nodes, the inverter pairs M16/M17 and M18/M19 invert the Ni node signal into a regenerated signal. These regenerated signals turn PMOS transistors M14, M12, M13, and M15 off. And eventually M6, M7, M20, M21 turns on. Hence the back-to-back differential pair again regenerates the Ni' node signals and because of M6 and M7 being on, the output latch stage converts the small voltage difference transmitted from Ni' node into a full scale digital level output.

E. Output Stage

The out+ and out- signals from M9/M11 and M8/M10 pairs respectively are combined in the output stage. These signals are given to two pass transistors. One pass transistor is driven by the analog input signal while the other transistor is driven by the inverted form of the input signal. The operation of a pass transistor is similar to an AND gate. The use of pass transistor reduces the number of transistors required for the AND operation. The outputs are the passed through individual buffer stages and then combined together.

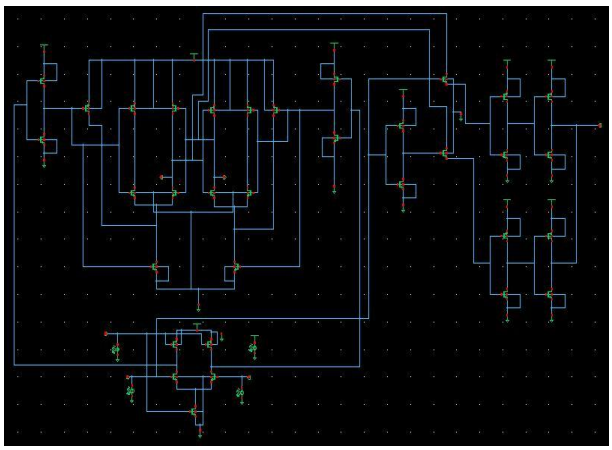

Fig.5. Schematic diagram of comparator

F. Layout

Fig.6. shows the layout of the comparator. The layout simulation is done using Cadence® Virtuoso Layout XL Design Environment. The DRC has been executed and compares with corresponding schematic of the comparator.

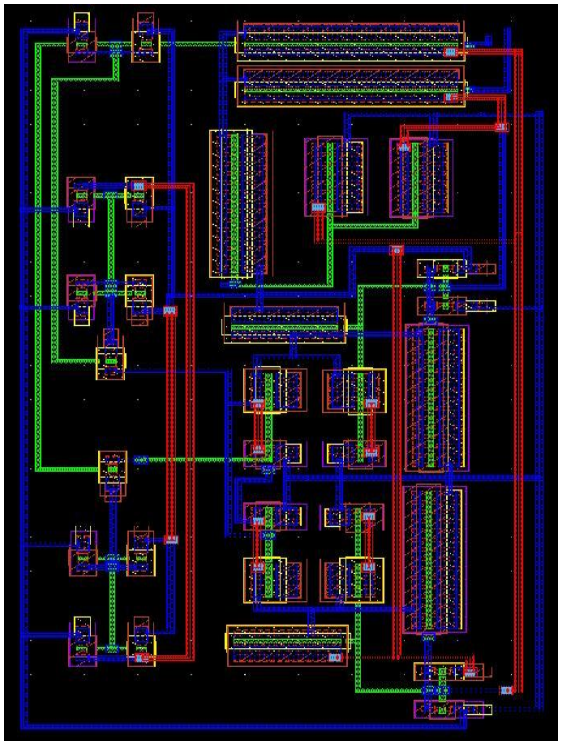

Fig.6. Layout of Comparator

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III. SIMULATION RESULTS

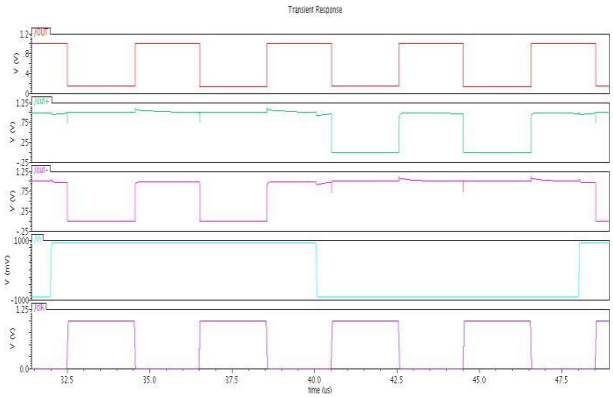

Fig.7. Comparator Waveform

Fig.7 shows the output waveforms during the schematic simulation of the comparator performed in Cadence® Virtuoso Analog Design Environment. During the positive half of the input analog signal, the switching is obtained at M9/M11 pair (out- pin) and during the negative half cycle of the input, switching is obtained at M8/M10 pair (out+ pin). The combined output is obtained at the output stage of the comparator.

The layout simulation is carried out in Cadence® Virtuoso Layout XL Design Environment. The Design Rule Check (DRC) and Layout Versus Schematic (LVS) were executed successfully without errors. The area of comparator layout was calculated to be 204.82 μm^2.

IV. DESIGN SPECIFICATION

Table I. Specifications Summary of Comparator

SUPPLY VOLTAGE	1V
TECHNOLOGY	CADENCE GPDK90nm
INPUT VOLTAGE RANGE	0V-0.9V
CLOCK FREQUENCY	250KHz
CLOCK RISE TIME	40 ns
CLOCK FALL TIME	40 ns
CLOCK PULSE WIDTH	2 µs
TEMPERATURE	27 °C
REFERENCE VOLTAGE	0.2V-0.7V
POWER DISSIPATION	44 µW
AREA	204.82 µm2

Table II. Transistor Dimensions

TRANSISTOR	WIDTH AND LENGTH (µm)	
	W	L
M1	4	0.1
M2	4	0.1
M3	4	0.1
M4	2	0.1
M5	2	0.1
M6	2	0.1
M7	2	0.1
M8	1	0.1
M9	1	0.1
M10	0.5	0.1
M11	0.5	0.1
M12	0.5	0.1
M13	0.5	0.1
M14	4	0.1
M15	4	0.1
M16	0.18	0.1
M17	0.18	0.1
M18	0.18	0.1
M19	0.18	0.1
M20	1	0.1
M21	1	0.1

V. CONCLUSION

A new dynamic comparator using positive feedback which gives better noise response, lower power dissipation than the conventional dynamic latched comparators has been proposed and targeted for ADC application. The results are simulated in Cadence® Virtuoso Analog Design Environment with GPDK 90nm technology. The back-to-back inverter is replaced with dual input single output differential amplifier in the latched stage. The transistor count in the output stage is reduced by using pass transistor logic.

REFERENCES

[1] Prasun Bhattacharya, "Design of a novel high speed dynamic comparatorwith low power dissipation for high speed ADCs,"National Institute ofTechnology Rourkela, Orissa, May 2011
[2] Pradeep Kumar, Amit Kolhe, "Design and Implementation of Low Power3-bit Flash ADC in 0.18µm CMOS,"International Journal of SoftComputing and Engineering (IJSCE), ISSN: 2231-2307, Volume-1, November 2011
[3] M. Miyahara, Y. Asada, P. Daehwa and A. Matsuzawa, "A Low-NoiseSelf-Calibrating Dynamic Comparator for High-Speed ADCs," in Proc.A-SSCC, pp.269-272, Nov. 2008.
[4] Jan M. Rabaey, "Digital integrated circuits - asign perspective," 2nd edition.
[5] BehzadRazavi, "Design of analog CMOS integrated circuits," New York, NY: McGraw-Hill, Inc., 2000